# LART: flexible, low-power building blocks for wearable computers

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## Abstract

*To ease the implementation of different wearable computers, we developed a low-power processor board (named LART) with a rich set of interfaces. The LART supports dynamic voltage scaling, so performance (and power consumption) can be scaled to match demands: 59-221 MHz, 106-640 mW. High-end wearables can be configured from multiple LARTs operating in parallel; alternatively, FPGA boards can be used for dedicated data-processing, which reduces power consumption significantly.*

## 1. Introduction

Small battery-powered wearable computers integrate the wearability and ubiquity of mobile phones with the computational capacity and flexibility of general-purpose computers. Furthermore, wearable computers equipped with sensors that monitor the environment and state of its user will offer *context aware* services to users. A straightforward example is location awareness for tourist and way-finding applications.

The rapid advances in technology will enable the production of quite powerful wearable computers in the near future. It is, however, unclear what the killer application, if any, will be. This depends on many factors. What user interface will become standard (PDA-style touch screens, or futuristic augmented reality glasses)? What infrastructure will telecom operators provide (proprietary information, or open access to public databases)? Will people collaborate through their wearables? These, and other questions have a serious impact on the requirements put on wearable computers.

The rapid development and uncertainty in the application domain calls for flexible hardware that can easily be reprogrammed, configured, and adapted to future needs. Unfortunately, flexibility can lead to inefficient usage of resources. The scarcest resource in a wearable is the battery, and flexible computing on a general-purpose CPU dissipates a lot more power than a static solution implemented in custom hardware.

This paper describes an approach that tries to strike a balance between flexibility and energy consumption. It combines general-purpose processing (on a low-power embedded StrongARM CPU) with FPGAs for dedicated signal processing and custom hardware to realize flexible high-end wearable computers dissipating modest amounts of power.

## 2. LART

At Delft University of Technology we are researching and developing wearable computers. They range from PDA-style devices handling multimedia information streamed over a wireless link to futuristic augmented reality terminals displaying visual information projected over and properly integrated with the real world. To minimize development effort – both hardware and software – we decided to use a general-purpose CPU as the core of all our wearables. We put a number of requirements on the processing core:

1 It must easily interface to wearable-specific devices like displays, sensors, and RF units.
2 It must be high-performance to support computationally intensive applications ($\geq$ 100 MIPS). Less demanding applications, however, should be supported efficiently as well.
3 It must be low-power ($\leq$ 1 W).
4 It must be supported by standard programming and debugging tools.
5 It must be an open system, such that research results can be made publicly available.

To solve the tension between high-performance and low-power we have adopted a modular approach. Each module is based on an embedded processor, which interfaces easily to the outside world, with modest performance and a good performance-to-power ratio. When needed a wearable can be configured as multiple units operating in parallel to deliver the raw MIPS required.

By equipping modules with different peripherals (e.g., position sensors, touch screen, LCD) we have realized a set of building blocks. The first wearable computer designed from these flexible, low-power building blocks was named the Linux Advanced Radio Terminal (LART) [1]. In Section 3 we detail the functionality and performance of the LART building blocks; the important low-power aspects are discussed separately in Section 4.

## 3. Building blocks

The LART is built around the embedded Intel SA-1100 StrongARM processor, which was selected for its low power/MIPS ratio and rich built-in peripheral support. It runs at 190 MHz with a performance comparable to a Pentium 180. The ARM processor is supported by the Linux operating system, which is very convenient since it comes with mature GNU utilities (e.g., gcc), and the modular structure and openness of Linux allows for easy extension and tailoring of device drivers. The support by Linux addresses requirements 4 and 5 on the StrongARM as stated in the previous section.

Figure 1 shows the LART processor board (7.5×10 cm) holding the CPU, 32 MB of EDO DRAM, 4 MB of Flash boot ROM, and various connectors. A PCMCIA adapter board has been developed for the LART to allow the use of standard expansion devices, such as WaveLAN wireless communication boards. At full speed the processor board consumes around 1 W (requirement 3). However, we have implemented frequency/voltage scaling (see Section 4.1), so applications requiring less than peak performance may consume less power. In other words, the performance and power dissipation of the StrongARM CPU can be matched to the needs of the application (requirement 2).

The SA-1100 processor has a built-in LCD interface. Other parts of the user interface are provided by a separate extension board, known as the Kitchen Sink Board (KSB), which includes the following:

- PS/2 interface (2×) for keyboard and mouse
- Stereo 16-bit 44 k1 audio out
- Mono 12-bit 26 k audio I/O (speakers + mic)
- Four channel 10-bit A/D converter
- USB client
- IrDA
- IDE channel and connector for 2.5” hard disk

Additionally, the Kitchen Sink Board offers a buffered databus to an optional 10Base-T Ethernet (4×) card. The rich set of supported interfaces (requirement 1) is enough to build PDA-style wearable computers. Ubicom’s augmented reality terminal [5], however, requires additional interfaces. We are developing boards for positioning (i.e. reading and processing sensor data from accelerometers, gyros, etc.) and rendering stereo images for a head-mounted display.

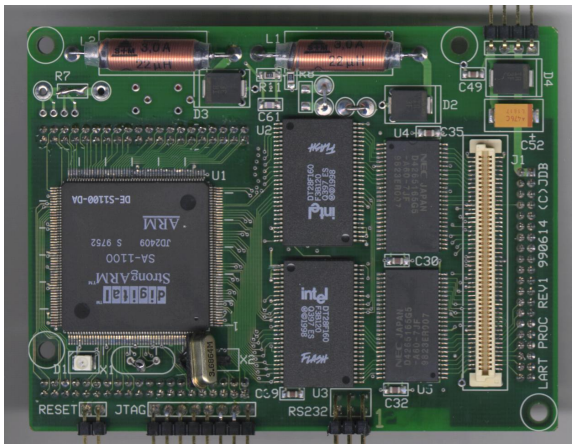


**Figure 1. LART – processor board.**

An interesting board (under development) is the extension board that holds an FPGA chip. It serves two purposes:

1. It offers a better power/MIPS ratio than the SA-1100 CPU for dedicated data-processing applications, like video capturing software (i.e. compression).
2. It can be programmed to interface two bi-directional high-speed serial (LVDS) links, which can interconnect multiple LARTs operating in parallel.

Cascading multiple LART boards is essential when the total processing requirement exceeds the capacity of a single StrongARM. Furthermore, it may ease the implementation of a wearable when different tasks are mapped onto separate processor boards: no contention for hardware resources (e.g., the single PCMCIA slot), no complicated scheduling of (conflicting) real-time requirements, etc. Table 1 lists three methods that can be used to connect multiple LART boards together. Energy per transferred bit is shown, both for the dynamic component only (dynamic) and the static plus dynamic consumption when running the link at full speed (total). The transfer energy over the (local) memory bus is shown for reference. All figures are for a complete link, including transmitter, cable capacitance,

| | speed | static power [mW] | energy per bit [nJ] dynamic | total |
|---|---|---|---|---|
| RS232 | 115 Kbps | 10 | 3 | 90 |
| Ethernet | 10 Mbps | 250 | 0.95 | 25 |
| LVDS | 700 Mbps | 300 | 0.05 | 0.5 |
| LVDS | 1.8 Gbps | 450 | 0.05 | 0.3 |
| Memory bus | 3.2 Gbps | - | 0.15 | 0.15 |

**Table 1. Interconnect characteristics.**

and receiver. Note that the transfer speed over the LVDS interface is adjustable: throughput can be traded for power consumption.

All schematics and design files of the LART building blocks are freely available through the web [2].

## 4. Low-power

Battery energy is the scarcest resource in a wearable computer. Therefore, LART components have been selected for low power. In the following sections we discuss low-power aspects of the LART designs.

### 4.1. Voltage scaling

The prime reason for selecting the SA-1100 processor is that it operates at a low voltage (1.5 V) and, consequently, dissipates (relatively) little power ($\leq$ 500 mW). Moreover, it supports frequency scaling and can operate at clock speeds ranging from 59 to 221 MHz, which has the potential of reducing the energy consumption. The necessary prerequisite is that the processor voltage must be reduced too; simply reducing the clock frequency does not pay off in comparison to switching the CPU on/off. Reducing the frequency *and* voltage does result in significant power savings due to the quadratic relation between power and voltage: $P \propto f \cdot V_{DD}^2 \cdot C$.

The data sheets specify that the SA-1100 operates only at 1.5 V, but experiments showed that a range of 0.8 V (at 59 MHz) to 1.5 V (at 221 MHz) is feasible. Since we want to dynamically adjust the frequency/voltage to match the processing demands of bursty applications, we have designed a programmable voltage regulator. We use some of the StrongARM's general-purpose I/O pins for this purpose. Note that only the voltage of the processor core (CPU + cache) is controlled, the other components (memory, buses, etc.) run from a fixed 3.3 V. The loss of the variable power supply was measured to be between 11% and 5% depending on the load, while the potential savings range up to 55%.

We extended the Linux kernel with a module that changes the clock frequency and core voltage. It also adjusts the memory parameters that control the read/write cycles on the external bus, because they are derived from the processor clock. The kernel module can be accessed from user-space by writing the desired frequency in the `/proc/scale` pseudo file; the kernel uses a lookup table to select the minimum core voltage at which the processor still functions for the selected frequency. The time needed to switch is 140 $\mu$s necessary to stabilize the internal clocks. This delay is low enough to support bursty applications with rapidly changing processing demands, for example, video decoding at 25 fps incurs a penalty of 0.35% (140 /$\frac{1}{25}$).

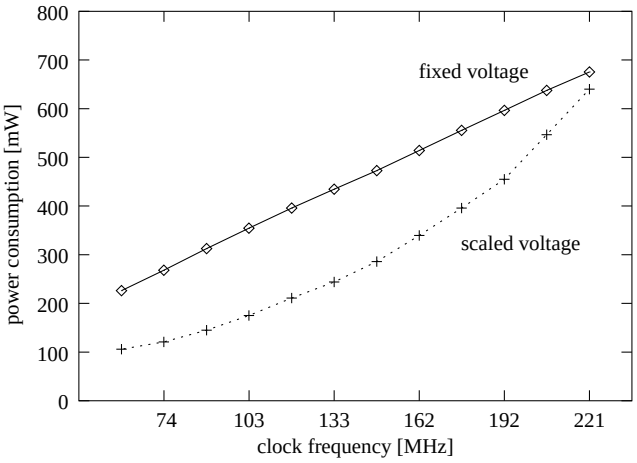


**Figure 2. Power consumption for Dhrystone.**

The effects of (static) voltage scaling are shown in Figure 2, which is taken from [6]. It plots the power consumption for the CPU-intensive Dhrystone benchmark when varying the processor frequency. When fixing the voltage (at 1.5 V), the power increases linearly with the frequency ('fixed voltage' curve). When scaling the voltage too, the resulting curve ('scaled voltage') shows the expected quadratic increase in power consumption. The difference is the largest at 74 MHz, in which case voltage scaling yields a factor 2.2 improvement. Note that voltage scaling will be less effective for real-world applications that exercise the memory subsystem (operating at fixed 3.3 V). For example, preliminary results obtained for an H263 video decoder show an overall power reduction of 25%, while the CPU power drops with 50%.

### 4.2. CreditLART

The configuration of the original LART requires external measurement and control equipment to support voltage scaling. Although dynamic (processor controlled) scaling is supported, it is only possible through an external D/A converter. While this setup supports power scaling research, it is not ideal. To support future low-power research within a more comprehensive, mobile experimental platform it is desirable to have a higher level of integration.

A new processing module has been developed to achieve this higher level of integration. This board, the CreditLART, uses newer technology than was available when the original LART was conceived, both in terms of components and PCB assembly. Modern assembly techniques allow the integration of LART and KSB functionality into one board; new semiconductor technology offers a lower power consumption than previous designs. By integrating a D/A converter the processor on the CreditLART is able to

directly control its own core voltage. In addition, current sensors on the major power rails allow the operating system to directly measure the power consumption of the system. The combination of these techniques enables power aware modules to obtain a better view of the state of the system.

Wherever possible the CreditLART component selection has taken power consumption into account. The (fast) memory bus is kept as short as possible, reducing capacitive load and thus power consumption. In memory-intensive applications this can save up to 100 mW. The power measurement and control circuits consume less than 1 mW. The power to major subsystems, such as audio and the hard disk, can be switched off. The power supply chips can be software-switched between high power and high efficiency.

### 4.3. Custom hardware

The LART system was designed with modularity and expandability in mind. One such expansion is the FPGA board mentioned in the Section 3. While primarily designed as an intelligent interface card for communication between LART boards, the FPGA on this board can also be used as a coprocessor in a wearable computer. The CPU can reconfigure the FPGA on the fly; since the footprint on the board can hold a wide range of Xilinx Virtex FPGAs, from cheap to high density (1 million gates) chips, this offers a flexible way to study the power impact of off-loading processing to a programmable chip.

We are also developing custom boards to assist wearables in specific tasks such as positioning and video capture. By customizing these boards power-efficient solutions can be obtained. As an example, we discuss the positioning system, which holds the following sensors:

- a 3D accelerometer (40 mW)
- a 3D gyroscope (90 mW)
- a 3D magnetometer (300 mW)
- a GPS receiver (600 mW)

The data from these sensors is fed through a Kalman filter that provides position estimates. In situations where power consumption is more important than position accuracy, it is possible to shut down these sensors for some period of time. Note that most sensors need some time to stabilize after power up. For example, the magnetometer normally provides 2000 samples per second and has a minimum stabilization time of 3 ms. If only 100 samples/sec are required, the sensor can be cyclically turned on for 3 ms and turned off for 7 ms, saving 210 mW.

## 5. Status

At the moment of writing only some of the LART modules described are fully operational: the LART processor and KSB boards. The others are in various stages of design, production, and debugging. We plan to put everything together in the first quarter of 2001. Our driving force is to demonstrate an augmented-reality system that is capable of rendering a statue in front of our university buildings. This requires the integration of a wireless link, positioning, and rendering into one wearable. Figure 3 shows the modular structure of the experimental platform. The positioning and wireless modules are LART-based, whereas the rendering module depends on graphics cards and accompanying software libraries only available for PC architectures. The positioning module was discussed in Section 4.3; the wireless module consists of a LART processor board, KSB, PCMCIA adapter board, and a standard WaveLAN card.

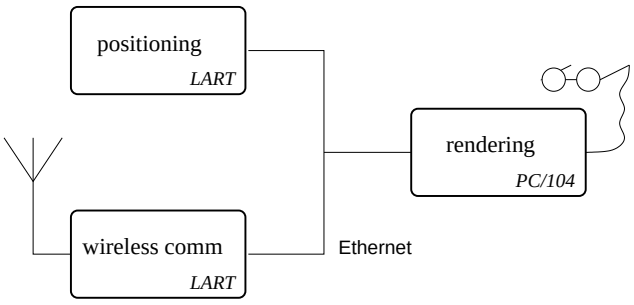


**Figure 3. Experimental platform architecture.**

The experimental platform (hardware + software + application) will allow us to study trade-offs between quality (performance) and cost (power consumption) in a realistic setting.

## 6. Related work

PDA-style devices are abundant in the consumer market. Almost all of them use low power components, some have quite powerful processors. As an example, the Compaq iPAQ H3600 series pocket PC has a design that is quite similar to the CreditLART, for once, it is also StrongARM based. Unfortunately PDAs that are commercially available tend to be closed designs, with little or no possibility to enable research by adding or change hardware.

PC/104 boards [4] are small (10×10 cm) and support standard interfaces (e.g., ISA and PCI), so they can interface with all sorts of peripherals. These characteristics make them quite popular among wearable computer researchers [7]. Unfortunately, PC/104 products do not offer much leeway when it comes to power consumption research. Furthermore, even 'low-power' PC/104 computers with comparable processing power consume over 5 W - versus 1 W for the LART.

The device that resembles the LART the most is the Itsy by Compaq [3]. Like the LART it is based on the StrongARM and targets the research community. The hardware designs, however, are not completely open: the use is restricted to internal, non-commercial research projects; Compaq reserves the right to use all derivative works the customer creates, royalty-free. An important technical difference is that the (linear) core power supply for the Itsy is by design tens of percents less efficient than the (switched) core supply of the LART. This difference can amount to over 200 mW consumed battery power

## 7. Conclusions

At Delft University of Technology we are implementing a wide range of wearable computers. To minimize design and implementation effort we have developed a set of flexible, low-power building blocks that can be used to configure individual wearables. The LART processor board, holding a low-power embedded StrongARM CPU, forms the heart of each wearable. We implemented voltage scaling, so that the CPU performance (and power consumption) can be matched against the demands of the application. If one CPU does not provide sufficient compute power, multiple LARTs can be interconnected to operate in parallel.

In addition to general-purpose processing, we are developing FPGA boards that provides a better power/MIPS ratio for dedicated data-processing applications. We will use it for video capture and as an interface to high-speed links forming the interconnect between multiple LARTs. By varying the clock frequency of the FPGA board, its performance can be matched to the demands, while reducing the power consumption considerably.

Finally, we are developing custom boards to assist wearables in very specific tasks such as positioning and video capture. In the case of the positioning board, which combines data from various sensors to yield an (accurate) location of the user, we again designed for flexibility. By varying the rate at which sensor data is processed, a trade-off between accuracy and power consumption can be made.

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